LIST OF INVENTORS' NAMES AND ADDRESSES

1.   Yusuke KANNO, Tokyo, Japan.

2.   Kiyoo ITO, Tokyo, Japan.

Title of the Invention

SEMICONDUCTOR INTEGRATED CIRCUIT

Inventors

Yusuke KANNO
Kiyoo ITO

SEMICONDUCTOR INTEGRATED CIRCUIT

BACKGROUND OF THE INVENTION

The present invention relates to a
semiconductor integrated circuit device, or in
particular to a technique for mounting a large-capacity
5 memory and a logic circuit on the same chip.

The references cited in this specification
are listed below and will be referred to with the
reference numbers attached thereto: Reference 1, "Very
Large Scale Integration Memory" by Kiyoo Itoh,
10 published by Baifukan Co., Ltd., 1994, pp. 13, and
Reference 2, JP-A-62-226494 (corresponding to US Patent
No. 4803664).

In recent years, the importance of a system-
on-chip LSI having mounted thereon both a dynamic
15 random access memory (DRAM) and a logic circuit at the
same time has increased for multimedia applications.
In the future, it will become necessary to mount a
DRAM, a static random access memory (SRAM) and a
processor or the like on a single chip. With the
20 conventional DRAM memory cell configured with a
transistor and a special large-capacity capacitor,
however, the process for fabricating the capacitor is
so complicated that it is difficult to fabricate the
DRAM through the same process as the logic circuit in a
25 system-on-chip LSI. The result is a limited cost

reduction. Thus a DRAM memory cell free of a capacitor is required.

Candidates are the 4.5, 3.5, 3.5 and 2.5 line-type 3-transistor cells shown in Figs. 1.0 (a) to

5 (d) on page 13 of Reference 1, for example, which the present inventors have begun to re-evaulate. The 3-transistor cell comprises a storage MOSFET for storing an information voltage in the gate thereof, a write MOSFET for writing the information voltage in the

10 aforementioned gate, and a read MOSFET for reading the state of the aforementioned gate voltage. The 3-transistor cell, which can be easily fabricated with substantially the same process as the logic circuit, may be fabricated at low cost. Also, this cell itself

15 has an amplification function, and therefore the operation is stable as a large read signal voltage is read on a data line. Further, this cell is suitably operated at low voltage and therefore can be implemented with low power consumption constituting a

20 suitable application to multimedia. These features have been discovered by the present inventors.

The DRAM comprising the 3-transistor cell is described also in Reference 2. This memory has a pair of data lines and is accessible for write and read

25 operation at high speed. In view of the fact that the information stored in the memory cell is detected and amplified by a sense amplifier, however, a dummy cell is required for each pair of the data lines, thereby

requiring a correspondingly increased space. Also, the dummy cell disclosed in the cited Reference 2 has an amplification function, and therefore the reference voltage appearing on the data lines undesirably changes
5 with time. As a result, it is difficult to set the start timing of the sense amplifier and in some cases, the read information cannot be detected by the sense amplifier. This is by reason of the fact that an excessively slow setting of the start timing of the
10 sense amplifier reduces the differential voltage between the pair of the lines and makes unstable the operation.

SUMMARY OF THE INVENTION

Accordingly, an object of the present
15 invention is to provide a memory not including a dummy cell.

A typical example of the present invention will be described. The dummy cell is eliminated by setting a different precharge voltage for each of the
20 data lines making up the data line pair connected to memory cells having the amplification function. Also, the stable operation is secured by setting the reference voltage appearing on the data lines to a predetermined value. A specific example of the memory
25 cell having the amplification function is so-called the 3-transistor cell including three transistors.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1A shows a most basic configuration according to an embodiment of the invention, and Figs. 1B and 1C show operation waveforms thereof.

Fig. 2A is a diagram for explaining a configuration including a CMOS latch circuit, and Fig. 2B a diagram for explaining a sense amplifier of CMOS latch type having a power supply with a switch.

Fig. 3A is a circuit diagram of a 3-transistor DRAM having the same word line for read and write operations, and Fig. 3B shows a waveform for driving the word line.

Fig. 4A is a circuit diagram of a 3-transistor DRAM with a read word line and a write word line separated from each other, and Fig. 4B shows waveforms for driving the word lines.

Fig. 5 is a circuit showing the essential parts of a memory circuit included in a semiconductor integrated circuit according to an embodiment of the invention.

Fig. 6 shows waveforms for explaining an example of the write operation of the memory circuit of Fig. 5.

Fig. 7 shows waveforms for explaining an example of the read operation of the memory circuit of Fig. 5.

Fig. 8 is a diagram showing a layout of the connections around the memory cell of Fig. 5 according

to an embodiment of the invention.

Fig. 9A is a sectional view taken in line a-a' in Fig. 8, and Fig. 9B is a sectional view taken in line b-b' in Fig. 8.

Fig. 10A is a sectional view taken in line c-c' in Fig. 8, and Fig. 10B is a sectional view taken in line d-d' in Fig. 8.

Fig. 11 is a circuit showing the essential parts of a memory circuit included in a semiconductor integrated circuit according to another embodiment of the invention.

Fig. 12 shows waveforms for explaining an example the write operation of the memory circuit shown in Fig. 10.

Fig. 13 is a circuit showing the essential parts of a memory circuit included in a semiconductor integrated circuit according to still another embodiment of the invention.

Fig. 14 shows waveforms for explaining an example the write operation of the memory circuit shown in Fig. 13.

Fig. 15 is a diagram showing a layout of the connections around the memory cell according to the embodiment of the invention shown in Fig. 13.

Fig. 16A is a sectional view taken in line e-e' in Fig. 15, and Fig. 16B is a sectional view taken in line f-f' in Fig. 14.

Fig. 17A is a sectional view taken in line g-

g' in Fig. 15, and Fig. 17B is a sectional view taken in line h-h' in Fig. 14.

Figs. 18A, 18B show yet another embodiment of the invention, in which Fig. 18A shows an example using a sense amplifier as shown in Fig. 2B, and Fig. 18B shows an example using a sense amplifier as shown in Fig. 2A.

Fig. 19 shows operation waveforms for the write operation in Fig. 17A.

Fig. 20 shows operation waveforms for the write operation in Fig. 17B.

Fig. 21 shows a further embodiment of the invention.

Fig. 22 shows a method of arranging the global data lines according to an embodiment of the invention.

Fig. 23 is a method of connecting the blocks and the global data lines according to an embodiment of the invention.

Fig. 24 is a diagram for establishing the electrical balance of the global data lines according to an embodiment of the invention.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[Embodiment 1]

Fig. 1A shows the concept of the invention and a configuration of a pair of data lines in a DRAM with the operation timing. The pair of the data lines

(DL, DLB) are connected to a plurality of memory cells
(MC1 to MCn), a sense amplifier (SA) and a precharge
circuit. The memory cells are gain cells as described
later. The gain cell, when used with a N-type MOSFET

5   described later, is defined as a cell in which a data
line precharged to a high potential VDD can be
discharged completely to zero selectively in accordance
with the information stored in the memory cell. The
gain cell can of course be used also with a P-type

10 MOSFET, and in that case is defined as a memory cell in
which the data line precharged to 0 V can be completely
charged selectively to a VDD level. The data line pair
includes a data line DL used for reading data from the
memory cells and a data line DLB used for access at the

15 time of differential amplification. The data line DLB
is used also for writing and rewriting the data in the
memory cell. The feature of the invention resides in
that a different precharge voltage is set for each of
the pair of the data lines. Specifically, when used

20 with the N-type gain cell, for example, the precharge
voltage of the data line DL is set to VDD while the
precharge voltage of the data line DLB is set to a
lower VDD/2. The sense amplifier is a CMOS sense
amplifier of latch type as shown in Figs. 2A, 2B, for

25 example, and amplifies the differential voltage
corresponding to the information appearing between the
pair of the data lines to VDD at high speed. The sense
amplifier is activated by applying 0 V and VDD to the

terminals SAN, SAP, respectively, in Fig. 2A, and the
terminals SPE, SNE, respectively, in Fig. 2B.

The basic operation of the invention will be
explained with reference to Figs. 1B, 1C on the
5 assumption that a N-type gain cell is used. For
reading the information stored in the memory cells, the
first step is to precharge the data lines DL, DLB to
VDD and VDD/2, respectively, by the precharge circuit,
after which the precharge signal PC is set to low
10 level, and then one of the word lines is selectively
set to the read level ("WLR on" in the diagrams). As a
result, it is determined whether the potential of the
data line DL is held at the precharge level or
discharged to 0 V in accordance with the information
15 stored in the memory cells. Fig. 1B shows waveforms
produced in the case where the memory cell holds such
information as to discharge the data line DL. After
the lapse of time T1 during which the voltage of the
data line DL decreases from VDD/2 by Δ (sensitivity of
20 the sense amplifier), the sense amplifier SA is
activated to start amplification ("SA on" in Figs. 1B,
1C). Thus, the data line DL is amplified to 0 V and
the data line DLB to VDD at high speed. The
sensitivity Δ is determined by the offset voltage of
25 the sensor amplifier or the like and is about 100 mV.
Fig. 1C shows waveforms produced in the case where a
selected memory cell holds such information as to
maintain the data line DL at the precharge level. In

the case where the sense amplifier is activated after time T1, the data line DL is amplified to VDD and the data line DLB to 0 V at high speed. Specifically, the information stored in the memory cell can be accurately detected and read out by activating the sense amplifier the time T1 after activating the word line WL. The precharge voltage difference between the pair of the data lines, which is VDD/2 in the drawings, may alternatively be not less than Δ. Assuming that the precharge voltage difference between the pair of the data lines is Δ, the time T1 becomes shorter and an amplification at higher speed becomes possible. Further, in the case where the precharge voltage of the data line DLB is set to Δ instead of VDD/2 (i.e. VDD = 2Δ), the read voltage difference for each of the pair of the data lines also has the same value for binary information. This condition leads to the minimum value of the precharge voltage of the data lines DL and DLB, and makes it possible to reduce the precharge voltage of the data line DL to 2Δ (about 200 mV). The advantage obtained by setting the precharge voltage of the data line DLB to VDD/2, however, is that the circuit design is facilitated and the precharge voltage level can be controlled with high accuracy. The precharge voltage of the pair of the data lines (DLB and DL), therefore, is determined based on the trade-off between the required speed and the difficulty of circuit design. The aforementioned condition for the

precharge voltage ideally permits the minimum value of
the operating voltage VDD to be reduced to 2Δ in
principle. This is an example not necessarily
requiring the sense amplifier. Once the requirement of
5 the operating speed is satisfied, therefore, the
operating voltage can be set to 2Δ without providing
the sense amplifier.

   The write operation into the memory cell can
be performed by setting the word line selectively to
10 the write level (a high voltage such as VDH) ("WLW on"
in Figs. 1B, 1C). In the case where the write data is
different from the stored information voltage of the
memory cell as shown in Figs. 1B, 1C, for example, the
data lines DL and DLB are impressed with differential
15 voltages of opposite polarities for the write
operation. Also, in the rewrite operation, the data
read out is amplified and the resulting amplified
voltage is rewritten, as described later.

   As described above, according to this
20 invention, the precharge level of the data line DLB can
be used as a reference voltage for amplification.
Thus, the dummy cell is not required, and no space
increase is required unlike in the prior art. Also,
since the reference voltage is constant with time, the
25 sense operation can be stabilized.

   Figs. 3A, 3B and 4A, 4B show examples of the
gain cell applicable to the present invention, which is
a 3-transistor memory cell made up of N-type MOSFETs.

Reference characters QS, QW and QR designate a storage
transistor, a write transistor and a read transistor,
respectively. This memory cell holds the information
by writing data of VDD or 0 V corresponding to the
5   binary information in the gate of the transistor QS and
then turning off the transistor QW. The memory cell
shown in Fig. 3 has a single word line connected to the
write transistor and the read transistor. This memory
cell, though small in area, requires a ternary level as
10 a word line driving voltage. Specifically, as long as
the memory cell is not selected (no row is selected),
the voltage of the word line is fixed to VSS which is
normally 0 V, while an intermediate voltage VDL is
applied at the time of the read operation and a
15 sufficiently high voltage VDH is applied at the time of
the write or rewrite operation. The reason why the
word line voltage is set to the intermediate level at
the time of the read operation is in order to turn on
the read transistor QR while keeping the write
20 transistor QW off. Otherwise, the information charge
held in the gate of the transistor QS would leak to the
data line DLB by the read operation. For controlling
the word line voltage in ternary way as described
above, the threshold voltages of the transistors QR and
25 QW are required to be set properly. First, consider
the case of discharging the data line DL at high speed
by way of the transistor QR with the stored information
held at the time of the read operation, when the

transistor QW is not easily turned on and the
transistor QS is turned on. The threshold voltage
(Vtw) of the transistor QW is desirably as high as
possible and the threshold voltage (Vtr) of the

5   transistor QR as low as possible. Usually, therefore,
the threshold voltages of the two transistors connected
to the same word line are conveniently set to different
values. In the case where the voltage Vtw is
excessively high, however, the condition VDH $\geqq$ VDD +

10   Vtw is required to be met to write the voltage VDD into
the gate of the transistor QS, resulting in what is
called a voltage stress breakdown of the MOSFETs.
Thus, the maximum value that can be assumed by the
voltage Vtw has its own limitation. In the case where

15   the voltage Vtr is excessively low, on the other hand,
a multiplicity of the row unselected memory cells
connected to the data line DL come to be slightly
turned on by what is called the subthreshold leak
current, thereby hampering the normal read operation of

20   the selected cell. Thus, the minimum value that can be
assumed by the voltage Vtr has also its own limitation.
Normally, to turn off the transistor QR with the word
line voltage of 0 V as the row unselected voltage, the
threshold voltage Vtr of the transistor QR is required

25   to be not less than 0.5 V. This excessively high
voltage Vtr reduces the read operation extremely at the
read voltage of intermediate level. A method for
solving this problem is to set the row unselected level

(VSS) of the word line to a negative voltage instead of 0 V. Even in the case where the voltage Vtr is set to 0 V, for example, the transistor QR can be turned off during the row unselected period by biasing the voltage

5   Vss deeply to -0.5 V or more. In such a case, the effective gate voltage for determining the drive rate of the transistor QR is given as VDL - Vtr, which is higher by 0.5 V as compared with the case where the voltage VSS is 0 V and the voltage Vtr is 0.5 V,

10   thereby making a high-speed read operation possible. Further, for amplifying the data lines at higher speed, the parasitic capacitance of the data lines should be reduced. This is effectively achieved by hierarchical data lines described later. The threshold voltage of

15   the transistor QS is determined on condition that the transistor QS is turned on strongly with the gate voltage of VDD and turned off or slightly turned on with the gate voltage of 0 V. Normally, Vtr ≧ 0 V. An example of the operation of this memory cell will be

20   described in detail later.

In the memory cell shown in Fig. 4, the gates of the read and write transistors are connected to the read word line and the write word line, respectively. The information stored in the memory cell is read by

25   applying a read voltage (VDH) to the read word line, and the information is written or rewritten into the memory cell by applying a write voltage (VDH) to the write word line. The read voltage may be VDD as long

as the read rate is sufficiently high. This memory
cell has a larger area than the memory cell of Fig. 3,
but the voltage of the word line is not required to be
controlled in ternary fashion as described above.

5   Thus, the problem of low-speed operation caused when
setting the read voltage to the intermediate level is
obviated, and the drive circuit can be easily designed.
Also, the same threshold voltage can be employed for
the transistors QR and QW in principle, and therefore

10 the process cost for fabricating a plurality of MOSFETs
is reduced. Further, the high-speed operation can be
secured effectively even with a low operation voltage
VDD by reducing the voltage Vtr and setting a
unselected level to a negative voltage, as described

15 above. Also, as described above, it is effective to
reduce the parasitic capacitance of the data line.
[Embodiment 2]

        Fig. 5 shows a memory circuit according to an
embodiment as a specific application of the embodiment

20 described above. The elements and the circuit blocks
shown in Fig. 5 are formed and mounted on a single
semiconductor substrate (LSI) such as single crystal
silicon by the well-known production technique for the
semiconductor integrated circuit.

25   According to this embodiment, the data lines
have a hierarchical structure including pairs of the
local data lines DL (DL1 to DLn), DLB (DLB1 to DLBk)
for supplying and receiving data to and from the memory

cells, and pairs of the global data lines GDL (GDL1 to
GDLk), (GDLB1 to GDLBk) longitudinally extending in
parallel. Each pair of the global data lines is
connected to a plurality of blocks BLK (BLK11 to

5 BLKmk). Each block includes a pair of local data lines
connected with the memory cells MC (MC11 to MCn1) and
switching MOSFETs (QRT, QWT) for connecting the global
data line and the local data line. The switching
MOSFETs are controlled by block select signals RWC

10 (RWC1 to RWCm) generated by a peripheral circuit
(PERI). A given pair of the global data lines
described above are connected to a complementary common
pair of the data lines (IO and IOB) by decoding an
external input address (YADR) of the DRAM core (DRAMC)

15 with a Y decoder (YDEC) and driving the corresponding
switches QY1, QY2 with a corresponding Y driver (YDRV).
Each pair of the global data lines, though not
specifically limited, have a well-known differential
amplifier of CMOS latch type SA including P-type

20 MOSFETs Q1, Q2 and N-type MOSFETs Q3, Q4 as shown in
Fig. 2A. The sense amplifier SA is activated by
applying the ground potential VSS and the source
voltage VDD to the common sources SAN and SAP,
respectively. Also, the differential sense amplifier

25 shown in Fig. 3B has the P-type MOSFET connected to the
high-voltage power supply VDD and the N-type MOSFET
connected to the ground side of the differential
amplifier of latch type shown in Fig. 2A to control by

switching the amplification operation with the control
signals SPE, SNE. This sense amplifier, which
undesirably increases the space by the size of the
switch thereof, has the advantage that the driving
5 force is large since the power supply is connected by
the switch. This embodiment will be explained
hereinafter with reference to the case the sense
amplifier of Fig. 2A is used.

        As described above, this invention has the
10 feature that the high-speed amplification operation is
made possible by the hierarchical structure of the data
lines which can reduce the capacitance of the data line
pair driven directly by the sense amplifier. This is
by reason of the fact that the capacitance of the
15 diffusion layer of the MOSFET is larger than the
parasitic capacitance of the wiring layer metal and
therefore the parasitic capacitance can be effectively
reduced by reducing the number of the MOSFETs connected
to the same wiring. The reason why the differential
20 amplifier is used, on the other hand, is to prevent the
rash current which otherwise might be generated in the
transistors QR, QS at the time of writing into the
memory cell. In the case where the voltage VDD is
written into the node N1 of the block BLK11 among
25 others, for example, the transistor QS is turned on.
At the same time, the transistors QR and QW are also in
on state, and therefore the data line DL1 acquires a
path to the voltage VSS. As a result, the rash current

is undesirably generated in the transistors QR and QS
unless the data line DL1 is at 0 V. This poses the
problem, for example, at the time of the operation of
inverting the 0 information stored in the node N1 to
5   the 1 information (what is called the inverted
writing), for example. In the process, the data line
DL1 is at the precharged level, so that the rash
current undesirably flows in the transistors QR and QS
unless written differentially.

10   The local data lines DL and DLB have
precharge MOSFETs QP1 and QP2 controlled by the
precharge signal PC. During the precharge period, the
data lines DL and DLB are precharged to a source
voltage VDD (say, 1 V) and a voltage VDD/2 (say, 0.5 V)
15 one half as large. Also, the pair of the global data
lines GDL, GDLB are precharged to the VDD/2 level
during the precharge period by the precharge MOSFETs
QP3, QP4 controlled by the precharge signal PC.

            The memory array is configured with a
20 plurality of data line pairs and a plurality of word
lines (WL1 to WLmn, etc.) orthogonal thereto. In the
drawing, four word lines WL1, WLn, WLmn-n+1, WLmn are
illustrated as representative ones. By decoding an
external input X address (XADR) with an X decoder
25 (XDEC), one of the word lines is selectively driven by
the X driver (XDRV) (also called the word driver).
This drawing shows an example in which the X address
and the Y address are input without multiplexing, but

the number of address terminals can be reduced to one
half by multiplexing the addresses.

Each memory cell is arranged at the
intersection between a word line and local data lines
5 DL, DLB, and is configured with three transistors
including a storage MOSFET QS adapted to turn on or off
by the information voltage at the gate thereof when the
particular word line is selected, a read MOSFET QR for
reading the information held by the transistor QS and
10 transmitting it to the local data line DL, and a write
MOSFET QW for applying the write data from the local
data line DLB to the gate of the transistor QS.
According to this embodiment, the gates of the
transistors QS and QR are connected to the same word
15 line. The source-drain path of the storage MOSFET QS
is connected to the read MOSFET QR and the ground
potential VSS (0 V) described above.

The data are input and output to and from
outside of the DRAM core. The read switch SW is turned
20 on and the memory cell is read. Then, the stored
information transmitted to the lines IO and IOB is
output to the data output terminal DO through a main
amplifier and a data output buffer DOB. At the time of
write operation, on the other hand, the data input to
25 the data input buffer DIB from the data input terminal
DI is transmitted with a differential voltage to the
lines IO and IOB by turning on the write switch WSW and
written in the memory cell by the write operation

described later.

A power generating circuit (VGC) has the function of decreasing, with a regulator or the like, the voltage VDD input from an external source to form a
5 VDL power supply and the function of generating a VDH power supply by boosting the voltage VDL or VDD with a charge pump circuit or the like. The voltages VDL and VDH are used as a read level and a write level, respectively, of the word line described later. In the
10 case where the VDL power supply is required to be higher than the voltage VDD, the VDD voltage input from an external source is directly boosted or regulated and then boosted.

This embodiment has the feature that a
15 reference voltage level of the differential sense amplifier is generated without a dummy cell by combining a memory cell having the amplification function and a pair of the local data lines set to different precharge voltages.

20 Fig. 6 shows waveforms for the write operation of the memory cell according to this embodiment. The block BLK11 will be taken as an example. When the precharge signal PC reaches a high voltage VDH (VDH $\geq$ VDD + Vtw (where Vtw is the
25 threshold voltage of the transistor QW)), the local data lines DL and DLB are precharged to the source voltages VDD and VDD/2, respectively. In similar fashion, the pair of the global data lines (GDL, GDLB),

the common sources (SAN, SAP) of the sense amplifier SA
and the common IO lines (IO, IOB) are precharged to
VDD/2.

Once the precharge signal PC reaches 0 V, the
5 precharge MOSFET is turned off, and therefore the pair
of the lines described above assume a floating state
thus continue to hold the precharge voltage. Under
this condition, the write and read operations into and
from the memory cell are carried out. An explanation
10 will be given below of the write, read and refresh
operations of the memory cell in the case where the
word line WL1 and the column line YS1 are selected.
(1) Write operation

For writing the high voltage VDD or the low
15 voltage VSS corresponding to binary information 1 or 0,
respectively, into the storage node (N1) of the memory
cell MC1, a sufficiently boosted high voltage VDH is
required to be applied to the word line WL1. This
voltage VDH is required to satisfy the relation VDH $\geqq$
20 VDD + Vtw, where Vtw is the threshold value (say, 0.5
V) of the write MOSFET QW (VDH = 2.5 V, for example).
Under this condition, assume that one (RWC1) of the
block select signal lines (RWC) is selected. Then, the
differential voltage corresponding to the write data
25 input from the data input terminal D1 is applied to the
gate of the transistor QS through the corresponding
local data line from the global data line and written
into the memory cell MC11. It should be noted here,

however, that once the voltage VDH is applied to the
word line WL1, the information stored in the column
unselected memory cells not selected by a column select
signal which is arranged on the same word line is

5   destroyed. Specifically, the precharge voltage VDD/2
of the corresponding local data line DLB1 is
undesirably applied to the storage node in each column
unselected memory cell. In order to prevent this
information destruction, all the memory cells on the

10 selected word line are read beforehand and by
amplifying them with each sense amplifier, the
amplified voltage is rewritten in the respective memory
cells. In the selected memory cell MC11, however, the
amplified voltage is written in by replacing it with

15 the input data voltage from the common data line I0B.
Thus, the read operation is required in advance of the
write operation. This read operation will be explained
below. As described above, the word line voltage of
the memory cell in Figs. 3A, 3B is required to be at

20 the ternary levels, including voltage VDL for reading,
the voltage VDH for writing and the voltage VSS for no
row selection.

         First, an explanation will be given of the
operation of reading the high voltage VDD which may be

25 stored in the memory cell MC11. The read operation is
started by applying a pulse of intermediate level
voltage VDL to the word line. The amplitude VDL of
this pulse is required to be set in such a manner as to

turn on the transistor QR and to turn off the transistor QW. For this purpose, the following conditions are required to be met.

5   Assume that the memory cell stores the binary information of voltage VDD or 0 V in the gate of the transistors QS and the stored information is detected according to whether the transistor QS is on or off when a read pulse is applied to the word line. For applying the read pulse VDL and turning on the

10 transistor QR, the following relation is required to be satisfied.

$$VDL > Vtr \qquad\qquad (1)$$

where Vtr is the threshold value of the transistor QR. If the information stored in the gate of the transistor

15 QS is not to be destroyed upon application of a read pulse to the transistor QW, the following conditions must be met. Specifically, the conditions for turning off the transistor QW are determined which assure that the charge accumulated in the gate of the transistor QS

20 is not released to the local data line DLB1 through the transistor QW in the case where the gate voltage of the transistor QS is VDD. The data line precharged to VDD/2 is the source of the transistor QW, and therefore the condition is described as follows.

25      $$VDL < VDD/2 + Vtw \qquad (2)$$

where Vtw is the threshold value of the transistor QW. In the case where the gate voltage of the transistor QS is 0 V, on the other hand, the transistor QS remains

off even if the gate of the transistor QS is charged
and the gate voltage is boosted from 0 V by the turning
on of the transistor QW, if the boosted voltage is
lower than the threshold voltage Vts. The condition
for this is as follows.

$$VDL < Vts + Vtw \qquad (3)$$

If the charge accumulated in the gate of the transistor
QS is not to be released to the local data lines for a
long time (say, 2 ms to 64 ms), the threshold voltage
Vtw is desirably increased. For high-speed reading, on
the other hand, the voltages Vts and Vtr are desirably
as low as possible. Thus, the threshold values of
these three voltages can be freely selected within a
range satisfying the aforementioned inequality.
Nevertheless, the voltage Vtr cannot be reduced as much
as the voltage Vts. Otherwise, an instability may be
caused. The reason is that a leak current (what is
called the subthreshold current) flows in the
transistor QR in a multiplicity of other unselected
memory cells connected to the same local data line
thereby reducing the precharge voltage of the local
data line. Assuming that VDD = 1 V, Vtw = 1 V, Vts = 0
V and Vtr = 0.5 V, for example, the range of the
voltage VDL in which the stored information is not
destroyed by the transistor QW is given as follows from
equations (1) to (3).

$$1.5 \text{ V} > VDL > 0.5 \text{ V}$$

By setting the voltage VDL in this way, the

data lines DL1 and DLB1 thus far precharged to VDD and VDD/2, respectively, are changed as follows. In the case where the gate (storage node N1) voltage of the transistor QS is VDD, the data line DL1 is discharged

5 to 0 V (designated by N1 in Fig. 6). Since the transistor QWT is in off state, the data line DLB1 is maintained at the precharge level VDD/2. In the case where the gate (storage node N1) potential of the transistor QS is 0 V, on the other hand, the transistor

10 QS is off and therefore the data line DL1 holds the precharge level (designated by N1' in Fig. 6). Since the transistor QWT is in off state, the data line DLB1 is maintained at the precharge level VDD/2. As already explained with reference to the first embodiment, the

15 high-speed read operation can be effectively accomplished by setting the row unselected level of the word line at a negative voltage and the voltage Vtr at a value as low as 0 V.

Now, after the stored information is read out

20 on the local data line DL1, assume that the control signal RWC1 is set to high level thereby to turn on the transistors QRT and QWT. The data lines DL1 and GDL1 or the data lines DLB1 and GDLB1 are connected to each other. In the process, the data lines DLB1 and GDLB1

25 are at the same potential level (precharge level), and therefore the potential remains unchanged. Nevertheless, a read signal (vs) appears on the data line GDL1 due to the charge share corresponding to the

parasitic capacitance as described below.

In the case where the local data line DL1 is discharged to 0 V, the level of the global data line GDL1 is reduced by vs from VDD/2, and the data line DL1

5 also comes to assume the same level, i.e. VDD/2 less vs. In the case where the read data line DL1 remains at the precharge level VDD, on the other hand, the data line GDL1 increases by a small voltage (+vs) from the precharge voltage VDD/2, and the data line DL1 also

10 comes to assume the same level of VDD/2 + vs. This situation is described by dotted line in the waveform diagrams of the data lines DL1, DLB1, GDL1, GDLB1 of Fig. 6, and designated by dashed symbols DL1', DLB1', GDL1', GDLB1', respectively. In this way, the small

15 read signal of -vs or +vs for VDD/2 appears on the global data line GDL1 in accordance with the binary information (1 or 0) held in the storage node of the memory cell. These voltages can be detected and amplified by the sense amplifier based on the precharge

20 voltage VDD/2 of the other global data line GDLB1. In the case under consideration, an explanation will be given of the case using a sense amplifier as shown in Fig. 2A. This amplification operation is carried out by increasing the common source line SAP to a high

25 voltage such as VDD and reducing the common source line SAN to a low voltage such as VSS. As a result, the global data line GDL is reduced to low level (VSS), while the other global data line GDLB1 complementary

with the data line GDL1 assumes a high level (VDH). As described above, this invention has the feature that the dummy cell which has conventionally been an essential part can be eliminated for amplification of

5   the information stored in memory. By the way, the control signal RWC1 can be raised to high level as soon as the precharge signal PC is reduced to low level. In such a case, the cases of timing to be controlled are reduced and therefore the design is facilitated.

10   The differential voltage between VDD and VSS applied to the pair of the common data lines (IO, IOB) for writing in the memory cell after amplification in the sense amplifier is sent to the pair of the global data lines (GDL1, GDLB1) and the pair of the local data

15   lines (DL1, DLB1) by setting the column select line YS1 to high level selectively. (In the drawing, the behavior of the data line DL1' indicated by dotted line represents the case in which 0 V is stored in the gate of the storage MOSFET QS.) After that, the word line

20   level is raised to the write level VDH. As a result, the voltage of the write data line DLB1 is transmitted to the gate of the transistor QS in the memory cell MC11 thereby to complete the write operation. An amplified stored information voltage is rewritten in

25   other column unselected memory cells on the same word line.

        Upon completion of the write operation into the column selected memory cell and the rewrite

operation into the column unselected memory cells as
described above, the word lines WL1 and YS1 are reduced
to low level and the transistors QY1, QY2 are turned
off. Further, the precharge signal PC is set to high
5   level (VDH) so that each local data line pair and each
global data line pair are precharged in preparation for
the next memory access.

(2) Read operation

        Fig. 7 shows waveforms for the read
10 operation. In the read operation, like in the write
operation described above, the read signal of a row and
column selected memory cell is amplified by the sense
amplifier SA and output to a common data line pair, and
led out by way of the data output terminal DO. By
15 setting the row select level of the word line to a high
voltage VDH, a voltage corresponding to the read
information is rewritten for all of the column-selected
cells and the column unselected cells.

(3) Refresh operation

20   The refresh operation is performed in such a
manner that the column select line YS is left in
unselected state in Fig. 7 while the read/rewrite
operation for all the memory cells on the word lines is
performed for all the word lines.

25   Fig. 8 is a diagram showing a layout related
to the memory cells according to this invention. Fig.
8 shows four memory cells shown in Fig. 5 and the
transistors QRT, QWT. A part of the word line WL1

fabricated of polysilicon layer (POLY) or the like
forms the gate of the transistors QR, QW of the memory
cell MC11, and the polysilicon layer in the same layer
forms the gate (GQS) of the transistor QS. The local
5 data line pair (DL1, DLB1, etc.) is formed of the metal
of the same layer (M2), and the global data line pair
(GDL1, GDL1B) are formed of the metal of another layer
(M3). The contacts LCT shown in Figs. 9A, 9B connect
the diffusion layer and the gate to each other
10 directly. The source· of the transistor QS is impressed
with the voltage VSS. This contact LCT is formed of
one metal layer (M1) and shared by the adjacent memory
cell for reducing the size. As a result, the two
memory cells are arranged in the same mirror symmetric
15 relationship. The two line pairs are connected by the
MOSFET (QRT, QWT) having the gate constituting a part
of the polysilicon wiring or the like.

     To clarify the relation between the layers,
the sectional views taken in lines a-a' and line b-b'
20 of Fig. 8 are shown in Figs. 9A and 9B. Fig. 9A shows
the sectional view taken in line a-a' representing the
section passing through the local data line DL1 and the
global data line GDL1. Fig. 9B is the sectional view
taken in line b-b' representing the section passing
25 through the local data line DLB1 and the global data
line GDLB1. In these diagrams, two contacts LCT are
shown. Further, the sectional views taken in line c-c'
and line d-d' orthogonal to the sectional views taken

in lines a-a' and b-b', respectively, are shown in
Figs. 10A and 10D. Fig. 10B shows two contacts LCT.

[Embodiment 3]

5   In the second embodiment described above, a
sufficient timing margin is available in view of the
fact that the read and transfer MOSFET QRT and the
write and transfer MOSFET QWT are controlled by a
single signal RWC. Also, the electrical balancing
level of the pair of the data lines as viewed from the
10   sense amplifier is so good that a correspondingly
stabler, high-speed operation is possible. In view of
the need of wiring the power lines of the voltages VSS
and VDD/2 for each block BLK, however, the area may
increase in some cases.

15   Fig. 11 shows the case in which only the
voltage VDD is used for the precharge power supply of
the local data lines DL, DLB, the MOSFET QRT for
selecting the read block is controlled using the read
signal RC, and the write control signal WC is used for
20   controlling the MOSFET QWT for selecting the write
block, thereby using independent control signals for
the read and write operations. According to this
embodiment, as compared with the second embodiment, the
operating speed may be decreased due to the independent
25   control operations of the read signal RC and the write
signal WC. Nevertheless, the number of precharge power
lines for each block arranged in the memory array can
be reduced to one half, and thus the space can be

reduced.

Fig. 12 shows operation waveforms for the embodiment shown in Fig. 11. An explanation will be given taking as a typical example the case in which the

5 memory cell MC1 of the block BLK1 in Fig. 11 has been selected. The write operation is performed in substantially the same manner as in Fig. 6 except that the connection method is different for the pair of the global data lines and the pair of the local data lines.

10 In Fig. 6, the write and transfer MOSFET QWT and the read and transfer MOSFET QRT are controlled by being turned on/off at the same time using the same control signal RWC. According to this embodiment, in contrast, the data lines DL and GDL are connected using the

15 control signal RC1 only for the MOSFET QRT after the potential of the local data line DL reaches VSS (in the case where the potential of the storage node N1 is VDD) or reaches the precharge level VDD (in the case where the potential of the storage node N1 is 0 V). As a

20 result, the data lines DL and GDL, as explained with reference to Fig. 6, reach the level of VDD/2 - vs in the case where the storage node N1 is at VDD and reach the level of VDD/2 + vs in the case where the storage node N1 is at 0 V. After the potential of the global

25 data line GDL has been established in this way, the potential of the pair of the global data lines is amplified by activating the sense amplifier. After amplification by the sense amplifier, as explained with

reference to Fig. 6, transmission of write data from an
external source turns on the transistor QWT by raising
the control signal WC1 to VDH level, so that the write
data is transmitted to the local data line DLB. After
5   the write data is transmitted to the local data line
DLB, the potential of the word line is set to the write
potential level VDH, so that the write data is written
in the storage node N1 of the memory cell. At the time
of reading, the transistors QRT and QWT cannot be
10 turned on at the same time. This is by reason of the
fact that the precharge level of the local data line
DLB is VDD, and therefore if the transistor QWT is
turned on at the time of reading, a small positive
signal would be undesirably transmitted to the global
15 data line GDLB precharged to VDD/2, thereby making it
impossible to obtain an accurate reference potential.
Especially in the case where the storage node N1 is at
VDD, the accurate amplification operation may become
impossible depending on the magnitude relation with the
20 small positive signal +vs appearing on the global data
line GDL.

        In the read operation, the read signal for
the selected memory cell is amplified by the sense
amplifier SA and output to the pair of the common data
25 lines and led out from the data output terminal DO. By
increasing the select level of the word line to the
high voltage VDH, a voltage corresponding to the read
information can be rewritten for all the column

selected cells and the column unselected cells.

For the refresh operation, on the other hand, the column select line YS is kept in unselected state while the read/rewrite operation for all the memory cells on the word lines is performed for all the word lines.

[Embodiment 4]

In the embodiments described above, the pair of the local data lines connected to the pair of the global data lines constitutes only a selected block in the case of amplification by the sense amplifier. This configuration can reduce the number of the MOSFETs connected to the pair of the global data lines and makes possible a high-speed amplification operation with a small load capacitance. This is because the parasitic capacitance of the metal wiring is generally smaller than the parasitic capacitance generated by the connection of a multiplicity of MOSFETs. Nevertheless, it is sometimes more desired to save the number of the wirings than to achieve the high-speed amplification operation. A memory array having a reduced number of wirings according to an embodiment will be explained below.

Fig. 13 shows a memory circuit according to another embodiment of the invention. The feature of this embodiment lies in that the number of wirings is reduced by the write local data line (DLB) and the global data line GDLB doubling as each other and thus

eliminating the transistor QWT required in the second
embodiment. Thus, the transistor QW of Fig. 5 is
directly connected to the global data line GDLB. As a
result, as described later, signal lines other than the
5 data lines can be arranged on the memory array without
adding a wiring layer, and the limited wiring layer can
be effectively utilized.

Fig. 14 shows waveforms for the write
operation of the memory circuit shown in Fig. 13. As
10 explained with reference to Fig. 6, the read and write
operation for the memory is carried out after the
precharge signal PC is reduced to low level. In this
embodiment, too, the read operation is performed in
advance of the write operation. The only difference
15 from the configuration of Fig. 6 is the absence of the
data line DLB. As described already, the information
stored in the memory cell MC1 is read out as a signal
of different polarity by the global data line GDL1, and
amplified and detected by the sense amplifier based on
20 the voltage (VDD/2) of the other global data line GDLB1
paired with the global data line GDL1. After that, as
described above, the amplification voltage is replaced
by the voltage of external write data and written in
the memory cell MC1. At the same time, the original
25 stored information voltage is rewritten in the other
memory cells. The read operation and the refresh
operation are also carried out in a similar manner.

Fig. 15 shows a layout around the memory

cell. The four memory cells and the transistor QRT and
the transistor QWT shown in Fig. 13 are shown. The
memory cell MC1 is such that a part of the word line
WL1 fabricated of a polysilicon layer or the like forms
5 the gates of the transistors QR and QW, and the
polysilicon layer forms the gate of the transistor QS.
The local data line DL and the global data line GDLB
are wired with the metal of the same layer (M2), while
the global data line GDL and the signal lines (SIG1,
10 SIG2, etc.) such as the column select line are formed
of the metal of another layer (M3). The contact LCT
shown in Fig. 15 directly connects the diffusion layer
and the gate. The power from the power supply VSS is
applied to the source of the transistor QS, which is
15 formed with a single metal layer shared by the adjacent
memory cell to reduce the size. As a result, the two
memory cells are arranged in the mirror symmetric
relationship. The data lines DL and GDL are connected
by the MOSFET QRT having a part of the wiring of
20 polysilicon or the like as a gate. To clarify the
relation between the layers, the sectional views taken
in lines e-e' and f-f' of Fig. 15 are shown in Figs.
16A and 16B. Fig. 16A is a sectional view taken in
line e-e' passing through the read data line DL1 and
25 the global data line GDL1. Fig. 16B is a sectional
view taken in line f-f' passing through the global data
line GDLB1 and the signal line. In Fig. 15, two
contacts LCT are arranged. Further, the sectional

views taken in lines g-g' and h-h' orthogonal to the
sectional views taken in lines e-e' and f-f' are shown
in Figs. 17A and 17B. Two contacts LCT are shown in
Fig. 17B.

5 [Embodiment 5]

        Figs. 18A, 18B show an embodiment of the
invention intended to reduce the number of the
precharge power wirings in the array thereby to further
save the space. Fig. 18A shows the case where the
10 sense amplifier of Fig. 2B, for example, is used, and
Fig. 18B shows the case where the sense amplifier of
Fig. 2A, for example, is used. This embodiment has the
feature that the precharge power wiring for the pair of
the local data lines which has been required for each
15 block BLK in Fig. 5 is eliminated, and the precharge
power supply is shared by the pair of the global data
lines. Figs. 18A, 18B show the case having four
blocks, but the present invention can be implemented
with any number of blocks other than four. First,
20 reference is had to Fig. 18A. In Fig. 18A, the global
data line GDL and the local data lines DL (DL1 to DL4)
are precharged to the source voltage VDD during the
precharge period, while the global data line GDLB and
the local data lines DLB (DLB1 to DLB4) are precharged
25 to the half precharge level VDD/2 during the precharge
period. For this to be accomplished, all the control
signals RWC (RWC1 to RWC4) are required to be set to
high level (turned on) during the precharge period.

During the precharge period, the sense amplifier
activation signal SPE is set to high level and the
signal SNE is set to low level in order to eliminate
the rash current. The rash current which otherwise
5   might pose a problem during the precharge period is
generated in the event that the precharge voltages of
the data lines GDL and GDLB are not equal to VDD and
VDD/2, respectively. In the case where the sense
amplifier shown in Fig. 2A is used, for example, the
10   transistor Q4 is turned half on during the precharge
period and therefore the current undesirably flows from
the global data line GDL to the common source line SAN.

          The write operation according to this
embodiment shown in Fig. 18A will be explained with
15   reference to Fig. 19. The read operation is performed
in advance of the write operation according to this
embodiment. The read operation will be explained
taking the memory cell MC11 of the block BLK1 as an
example. In Fig. 19, the word line connected to each
20   memory cell is not shown. The data lines are
precharged when the precharge signal (PC) is at high
level. In the process, the pair of the global data
lines GDL, GDLB are precharged to VDD and VDD/2,
respectively. At the same time, the control signal
25   RWC1 is set to high level and the pair of the local
data lines is connected to the pair of the local data
lines DL1, DLB1 in order to precharge the pair of the
local data lines DL1, DLB1. As a result, the pair of

the local data lines DL1, DLB1 are precharged to VDD
and VDD/2, respectively. For starting the read
operation, the precharge is required to be stopped by
setting the precharge signal PC to low level. When the

5   precharge signal PC is at low level, the potential of
the word line is set to the read level VDL thereby to
start the read operation from the memory cell of a
selected row. In the process, the control signals RWC2
to RWC4 of the unselected blocks are desirably set to

10   low level as designated by RWC' in Fig. 19. By doing
so, the load capacitance on the pair of the global data
lines can be reduced. This is by reason of the fact
that the memory cell transistors of the unselected
blocks are electrically disconnected with the pair of

15   the global data lines, and therefore the load
capacitance can be reduced by an amount equivalent to
the parasitic capacitance due to the MOSFETs not
connected. After waiting until the read potential for
the local data line DL1 and the global data line GDL is

20   reduced below VDD/2, the sense amplifier activation
signal SPE is set to low level and the signal SNE to
high level, so that the sense amplifier is activated
and the read signal is amplified accurately to 0, 1.

         In the first step of the read operation for
25   the memory cell, the column select switches QY1 and QY2
are turned on so that the write signal voltage
transmitted to the pair of the common data lines is
transmitted to the pair of the global data lines.

After that, the word line is set to the write level VDH
so that the write signal is transmitted to the storage
node N1 of the memory cell. In this way, the word line
is set to the column unselected level of 0 V thereby to
5   electrically isolate the storage node from the local
data line. After that, the precharge state is restored
in the same manner as explained with reference to Fig.
2.

Reference is made to Fig. 18B showing a
10 modification of the embodiment explained with reference
to Fig. 18A. This modification has a different
configuration of the sense amplifier. The shown
configuration includes a sense amplifier having an
equal precharge level for the pair of the data lines
15 connected to the sense amplifier. The pair of the
global data lines GDL and GDLB shown in Fig. 18B have
the precharge level of VDD and VDD/2, respectively,
which are not equal to each other. In view of this, a
pair of main data lines MGDL, MGDLB having the
20 precharge level of VDD/2 and isolated by the isolating
MOSFETs Qi1 and Qi2 are newly provided and connected to
the sense amplifier to amplify the read signal.

With reference to Fig. 20, the write
operation according to the embodiment shown in Fig. 18B
25 will be explained. In this case, too, the read
operation is performed in advance of the write
operation. The read operation will be explained taking
the block BLK1 as an example. In Fig. 20, the word

line connected to each memory cell is not shown. The
data line is precharged when the precharge signal (PC)
is at high level. In the process, the pair of the main
data lines MGDL, MGDLB are precharged to VDD/2, and the
5 pair of the global data lines GDL, GDLB to VDD and
VDD/2, respectively. At the same time, in order to
precharge the pair of the local data lines DL1, DLB1,
the control signals RWC1 to RWC4 are set to high level
and the pair of the local data lines are connected to
10 the pair of the global data lines. As a result, the
pair of the local data lines DL, DLB are precharged to
VDD and VDD/2, respectively. For starting the read
operation, it is necessary to stop the precharge
operation, which is accomplished by setting the
15 precharge signal PC to low level. When the precharge
signal PC is at low level, the potential of the word
line is set to the read level VDL thereby to start the
read operation from the memory cell of a selected row.
In the process, the control signals RWC2 to RWC4 for
20 the unselected blocks are desirably at low level as
designated by RWC' in Fig. 20. By doing so, the load
capacitance on the pair of the global data lines can be
reduced. ~ Upon complete reading onto the local data
line DL1 and the global data line GDL, the control
25 signal IC is set to high level, and the read signal
voltage transmitted to the global data line is
transmitted to the main data line MGDL. As a result,
the charge share corresponding to the parasitic

capacitance of each data line causes the read signals
($\pm$vs) having different polarities corresponding to the
information voltage of the storage node to appear on
the main data line MGDL. Since the the data lines GDLB
5   and MGDLB have the same potential level (precharge
level), the potential remains unchanged. As described
with reference to Fig. 6, therefore, the read signal of
VDD/2 + vs or VDD/2 - vs is transmitted to the main
data line MGDL in accordance with the read signal from
10 the memory cell. After the read signal is transmitted
to the main data line MGDL, the control signal IC is
set to low level thereby to isolate the pair of the
main data lines MGDL, MGDLB and the pair of the global
data lines GDL, GDLB from each other. By thus
15 isolating the global data lines at the time of
amplification, the parasitic capacitance of the main
data lines MGDL, MGDLB is reduced and therefore high-
speed amplification is made possible. After that, the
read signal is accurately amplified to 0, 1 by the
20 sense amplifier connected to the main data lines.

        For the write operation into the memory cell,
the first step is to turn on the column select switches
QY1, QY2 so that the write signal voltage transmitted
to the pair of the common data lines is transmitted to
25 the pair of the main data lines MGDL, MGDLB, and the
control signal IC is set to high level, which control
signal IC is transmitted to the pair of the global data
lines by turning on the switches QI1, QI2. After that,

the write signal is transmitted to the storage node N1
of the memory cell by setting the word line to the
write level VDH, and the word line is set to the
unselected level of 0 V thereby to isolate the storage
5   node from the local data lines. Then, the precharge
state is restored in the same manner as described with
reference to Fig. 6. Incidentally, the precharge
MOSFET QP1 and the isolating MOSFET Qi1 have the same
precharge voltage for the data lines MGDLB, GDLB, and
10 therefore are not required basically. Nevertheless,
the advantage of the provision of these MOSFETs is that
the pair of the main data lines MGDL and MGDLB are kept
in electrical balancing level and therefore a stable
amplification operation can be realized.
15 [Embodiment 6]

       Fig. 21 shows still another embodiment in
which the precharge power supply is shared by the pair
of the local data lines and the pair of the global data
lines. This embodiment is equivalent to the memory
20 array configuration of the embodiment shown in Fig. 13
except that the precharge power wiring is shared by the
pair of the local data lines and the pair of the global
data lines. This embodiment is also different from the
embodiment of Fig. 13 in that the precharge level of
25 the global data line GDL is set to VDD. By the way,
the number of blocks is 4 in Fig. 21 to which the
invention is not limited but can be implemented with
other than four blocks.

The write operation and the read operation
are substantially the same as those explained with
reference to Fig. 14. Also, the operation for
controlling the write and read operation to and from
5   the global data lines is substantially the same as the
corresponding operation explained with reference to
Fig. 19. Specifically, the operation with the control
signals RWC, RWC' are replaced with the operation with
the read signals RC, RC' in Fig. 19, so that the
10 control operation is performed in accordance with the
operation waveforms not requiring the operation of the
data line DLB1.

[Embodiment 7]

In the memory array configuration shown in
15 Figs. 5, 10 and 13, the number of the MOSFETs connected
to the pair of the global data lines GDL, GDLB is not
uniform, and therefore the parasitic capacitance is
different between the global data lines GDL and GDLB.
As a result, an effective noise or a reduced operation
20 speed is often caused from the viewpoint of the sense
amplifier. Fig. 22 shows an embodiment in which the
pair line configuration for reducing the ununiformity
of the parasitic capacitance between the pair of the
lines is employed in the configuration of Fig. 13.
25 According to this embodiment, the pair of the global
data lines are twisted on the memory cell to obviate
the ununiformity of the capacitance between the pair of
the lines. Also, the noises generated in the global

data lines GDL and GDLB can be successfully offset by changing the manner in which each adjacent pair of the global data lines are twisted, as shown in Fig. 22.

First, an explanation will be given of the
5   equalization of the parasitic capacitance. For convenience' sake, adjacent pairs of the global data lines (GDL1, GDLB1 and GDL2, GDLB2) will be taken as an example. These global data line pairs each are assumed to be connected with four blocks each including n
10 memory cells MC11 to MC1n. Also, assume that the block BLK11 is selected and the control signal RC is at high level. Under this condition, the data line GDL1 is connected with a total of 3n + 2 transistors, i.e. (n + 1) MOSFETs including the transistor QRT of the block
15 BLK11 and the read MOSFETs connected thereto, n write MOSFETs for the BLK12, one read and transfer MOSFET for the block BLK13, and n write MOSFETs for the block BLK14. The global data line GDLB1, on the other hand, is connected with a total of 2n + 1 MOSFETs including n
20 write MOSFETs for the block BLK11, one read and transfer MOSFET for the block BLK13, n write MOSFETs for the block BLK13 and one read and transfer MOSFET for the block BLK14. In the case where the global data lines are not twisted, the number of the MOSFETs
25 connected to the global data line GDL is n + 4 in total including the transistor QRT of the block BLK11 and n read MOSFETs connected thereto, a read and transfer MOSFET for the block BLK12, a read and transfer MOSFET

for the block BLK13 and a read and transfer MOSFET for
the block BLK14. The number of the MOSFETs connected
to the global data line GDLB, on the other hand, is 4n
in total including n write MOSFETs for the block BLK11,

5 n write MOSFETs for the block BLK12, n write MOSFETs
for the block BLK13 and n write MOSFETs for the block
BLK14. In this way, the imbalance of the number of the
MOSFETs connected to the global data line pair is   .
remarkably improved. In similar fashion, the

10 arrangement of the pair of the global data lines as
indicated by the data lines GDL2, GDLB2 also equalizes
the number of connections on the read and write sides
of the block BLK and therefore clearly improves the
imbalance of the number of the connected MOSFETs.

15   Now, the reduction in the noise appearing in
the global data lines GDL and GDLB will be explained.
At the time of write and read operations of the memory,
the data lines GDL and GDLB change from the precharge
level to VDD or VSS. This process is known to generate

20 a noise in adjacent global data lines due to capacitive
coupling. In the case where the data lines GDL and
GDLB are arranged as shown in Fig. 22, the pair of the
global data lines (GDL2, GDLB2) of equal length are
arranged adjacently to, say, the data line GDL1, the

25 same noise comes to appear on the data lines GDL2 and
GDLB2. The same level of the noises generated in the
data lines GDL2 and GDLB2 eliminates the likelihood of
a malfunction at the time of amplification operation of

the sense amplifier.

Incidentally, the invention is not limited to this example in which a pair of global data lines are connected with four blocks.

5 [Embodiment 8]

Fig. 23 shows another embodiment in which the parasitic capacitance of the pair of the global data lines is maintained in equilibrium. In this embodiment, the read and transfer MOSFET is connected

10 to the global data line GDL2 of one half of the blocks (BLK11 and BLK13, for example) connected to the global data line pair. For the remaining one half of the blocks (BLK12 and BLK14, for example), a write MOSFET is connected to the data line GDL1, and a read and

15 transfer MOSFET is connected to the data line GDLB1. In the case where the block BLK11 is selected, therefore, $(3n + 2)$ MOSFETs are connected to the data line GDL1, and $(2n + 2)$ MOSFETs are connected to the GDLB1. This case uses a structure in which the pair of

20 the global data lines are not twisted to obviate the imbalance of capacitance. The twisting of wirings generally uses two or more metal wiring layers. According to this invention, therefore, the number of the wiring layers used can be reduced. Thus, space can

25 be saved by allotting the limited wiring layers to other signal lines and power lines. In the shown case, the blocks such as BLK11 and BLK12 connected to the adjacent global data line pairs are arranged in the

mirror symmetric relationship with respect to the
global data lines. Nevertheless, the arrangement in
mirror symmetric relationship is not necessarily
required, but the blocks can be arranged in any manner
5 determined from the viewpoint of the layout ease.
[Embodiment 9]

Fig. 24 shows waveforms for explaining still
another embodiment of the invention intended to
equalize the parasitic capacitance generated in the
10 data lines GDL and GDLB of the memory cell. The
embodiment of Fig. 13 will be taken as an example.
This embodiment relates to a method of controlling the
control signal for transmitting the information stored
in the memory cell to the global data lines. According
15 to this embodiment, the read data is transferred to the
global data line GDL by turning on the read and
transfer MOSFET by the control signal RC1, after which
the read and transfer MOSFET is turned off before
amplification in the sense amplifier. Since the n
20 transistors QR of the selected block are electrically
isolated from the data line GDL, the capacitance
involved fails to function as a load capacitance at the
time of operation of the sense amplifier. Thus, the
MOSFETs connected to the data lines GDL and GDLB
25 number 2n + 2, thereby further obviating the imbalance
of parasitic capacitance.

The present invention eliminates the need of
the dummy cell which has been essential to the

conventional DRAM circuit using the gain cell, and
therefore can reduce the required space and the
fabrication cost. Also, the hierarchical data line
structure makes high-speed operation possible.